Amendments to the Drawings:

The attached sheet of drawings includes changes to Figs. 1-5. These sheets replace the original sheets including Figs. 1 – 5. In all of the figures, the term "Figur" was replaced by "Figure". In Fig. 5, the boxes have been labeled.

Attachments: Replacement Sheets

Annotated Sheet Showing Changes

REMARKS/ARGUMENTS

The present amendment is submitted in response to the Office Action dated December 12, 2006, which set a three-month period for response, making this amendment due by March 12, 2007.

Claims 10 – 15, 17 and 18 are pending in the application.

In the Office Action, the drawings were objected to for an informality. The specification was objected to for various informalities and a substitute specification was requested. Claims 10-13 and 15 were objected to for various informalities. Claims 10, 13, and 15 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claims 10, 14, and 15 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,600,679 to Tanzawa et al. Claims 11-13 and 16-18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tanzawa et al.

In the present amendment, the figures have been amended to address the objections.

As requested, a substitute specification is included herewith, both in a marked-up version and as a "clean" version. In the substitute specification, the changes made to the specification in the previously filed Preliminary Amendment have been incorporated. In addition, the terms "inlet" and "outlet" have been changed to "input" and "output", respectively. The terms "capacity" and "capacities" were changed to "capacitance" and "capacitances", respectively. Likewise, the claims were amended to adopt the changes to these terms.

The title of the invention was amended to adopt the title proposed by the Examiner.

With regard to the claim objections, again, the objected-to terms were changed in the claims. Claim 13 was amended to depend on claim 11, rather than claim 10. Claim 15 was amended to clarify the "applied differential principle".

Regarding the objection raised under paragraph 8 in the Office Action (page 4), the Applicants respectfully disagree that the figures do not show the inputs to the inverters being complementary to each other. In Figs. 1 through 4, the inputs N1 and N2 are clearly shown as inputs: the inputs of the first inverter circuit (3) and the second inverter circuit (4), respectively, of the voltage transmitter (2), which are a non-inverted and inverted input, comprise two inverted circuits 3, 4, whose outputs are simultaneously the outputs of the voltage transmitter 2. The Applicants therefore submit that the limitation as recited in claim 10 is not indefinite.

Turning now to the substantive rejection of the claims, claim 10 has been amended to add the features of claim 16, which was canceled.

In contrast to the device shown in Tanzawa, with the present invention, the digital signal level can be made available with common voltage levels between approximately 3V to 15V via a potential differential up to several hundred volts (depending on the technology and application that are used) to another voltage level. Thus, the potential differential between the input voltage level, which is synonymous to the voltage transmitter, and the output voltage level, which is synonymous with the voltage receiver, vary positively or negatively as well as in the potential height. Thus, advantageously, any technologies for integrated high voltage circuits can be applied to any insulating methods to realize the circuit arrangements.

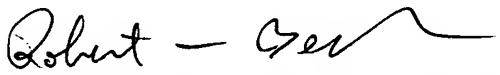
The capacitances C1 and C2 of Tanzawa et al are not described in detail. Therefore, amended claim 10 includes the limitations relating to the capacitances C1 and C2, specifically, that "*the circuit arrangement for bridging high voltage with a switching signal is realized as an integrated semi-conductor circuit made with semi-conductor processes with CMOS circuits as the inverter circuits or a stack of layers with alternating layers of circuit stopper implantation, field oxide, poly-silicon, CVD-oxide, metal, CVD-oxide, metal, and so on, whereby the layers are electrically alternatingly connected, as the first capacitor and as the second capacitor, respectively, as high voltage capacitors*".

Tanzawa et al do not disclose or suggest that the layers are alternatingly connected, that the inverter circuits are CMOS circuits, or that the high voltage capacitances as well as the inverter circuits are integrated semi-conductor circuits made with semi-conductor processes.

Because Tanzawa fails to disclose all of the features of amended claim 10, the rejection under Section 102 must be withdrawn. Tanzawa cannot be an appropriate reference either under MPEP section 2131, which indicates that to anticipate a claim a reference must teach every element of the claim in as complete detail as is contained in the Applicants' claim, or under MPEP section 2143.03, since not all of Applicants' claim limitations are taught or suggested

The application in its amended state is believed to be in condition for allowance. However, should the Examiner have any comments or suggestions, or wish to discuss the merits of the application, the undersigned would very much welcome a telephone call in order to expedite placement of the application into condition for allowance.

Respectfully submitted,



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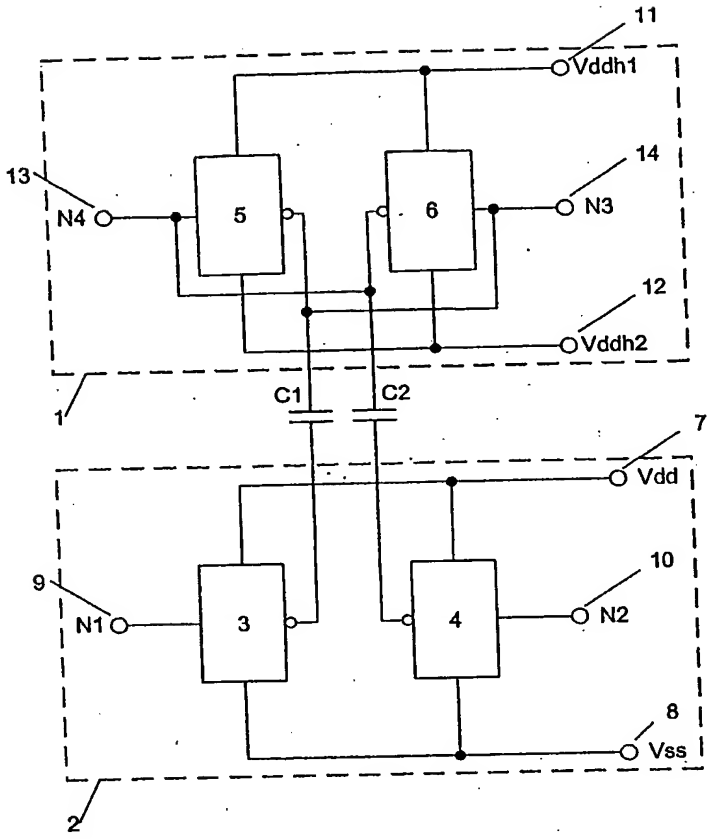
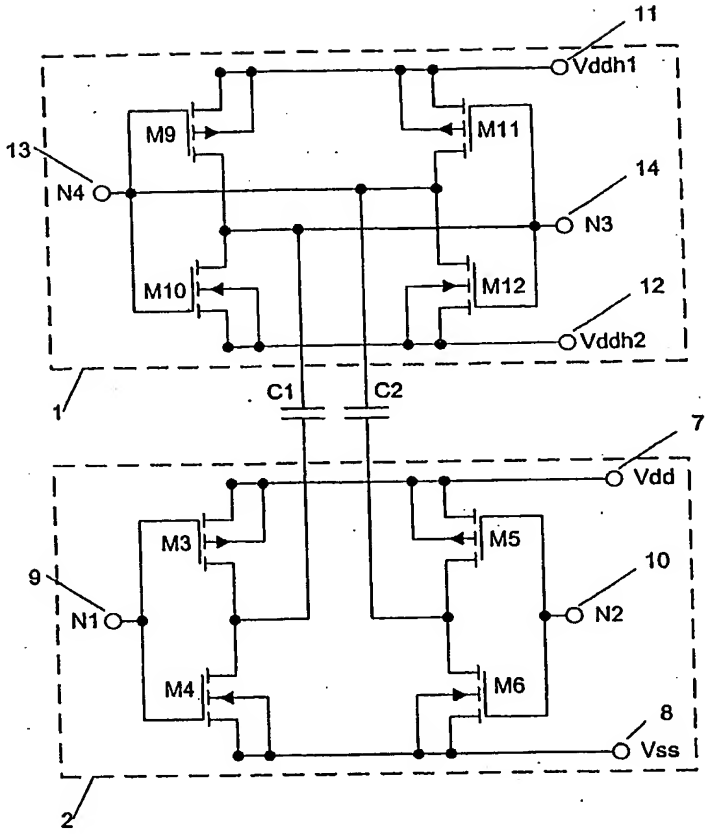
Attachments



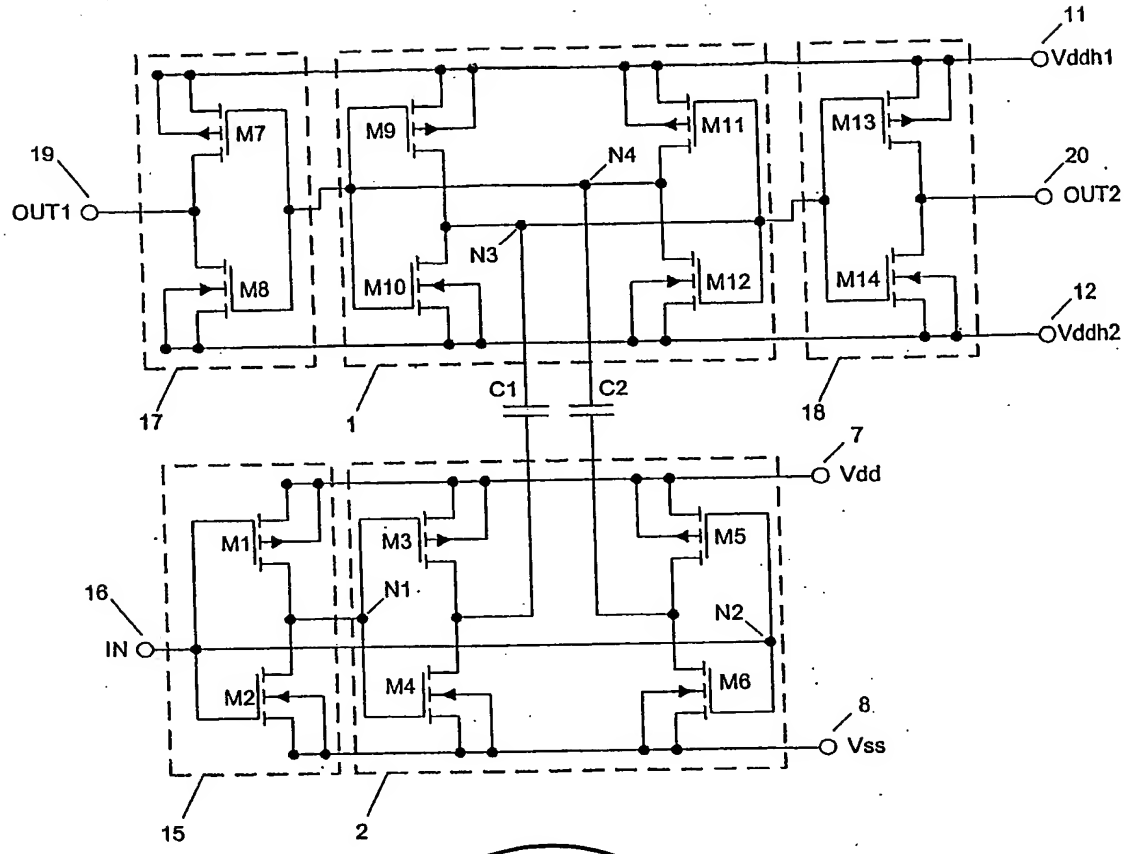
~~Figur 1~~

Figure 1



~~Figur 2~~

Figure 2



Figur 3

Figure 3

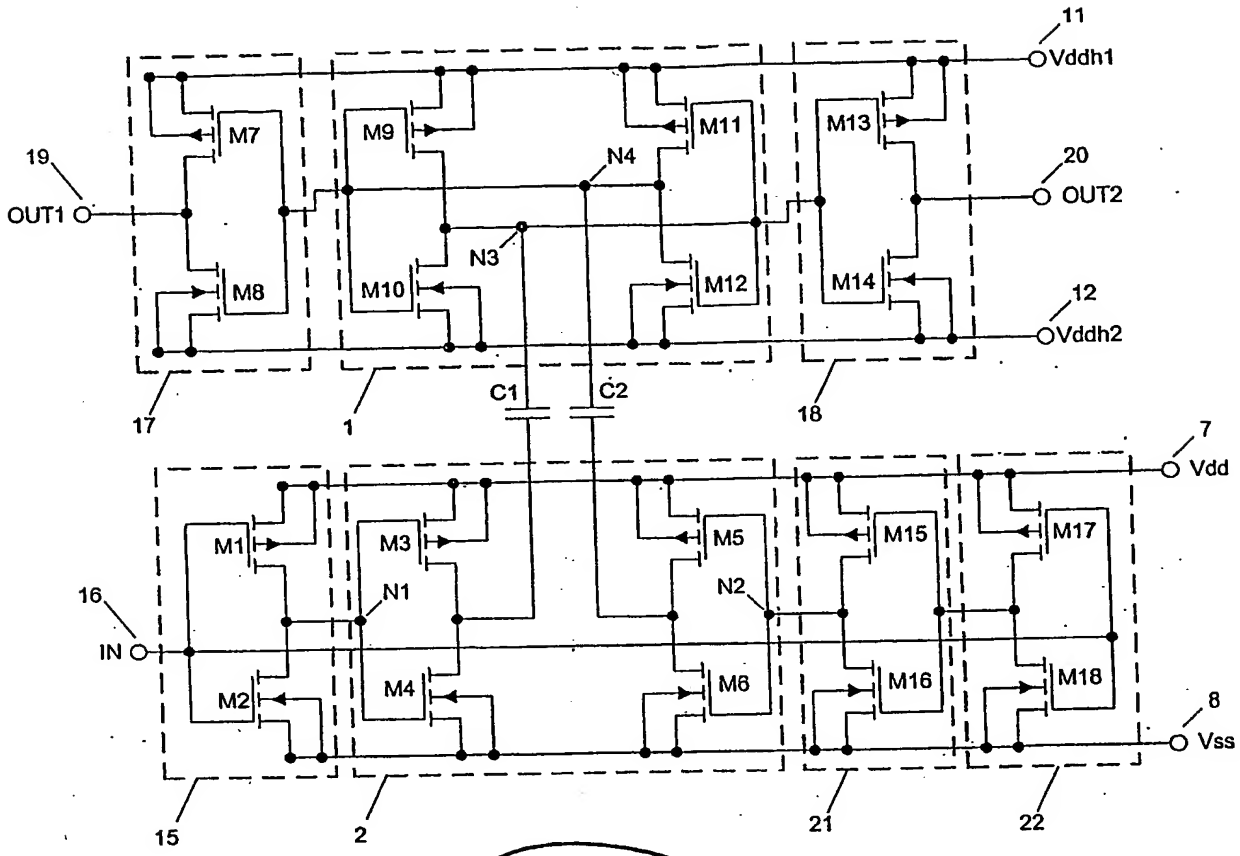


Figure 4

~~Figur 4~~

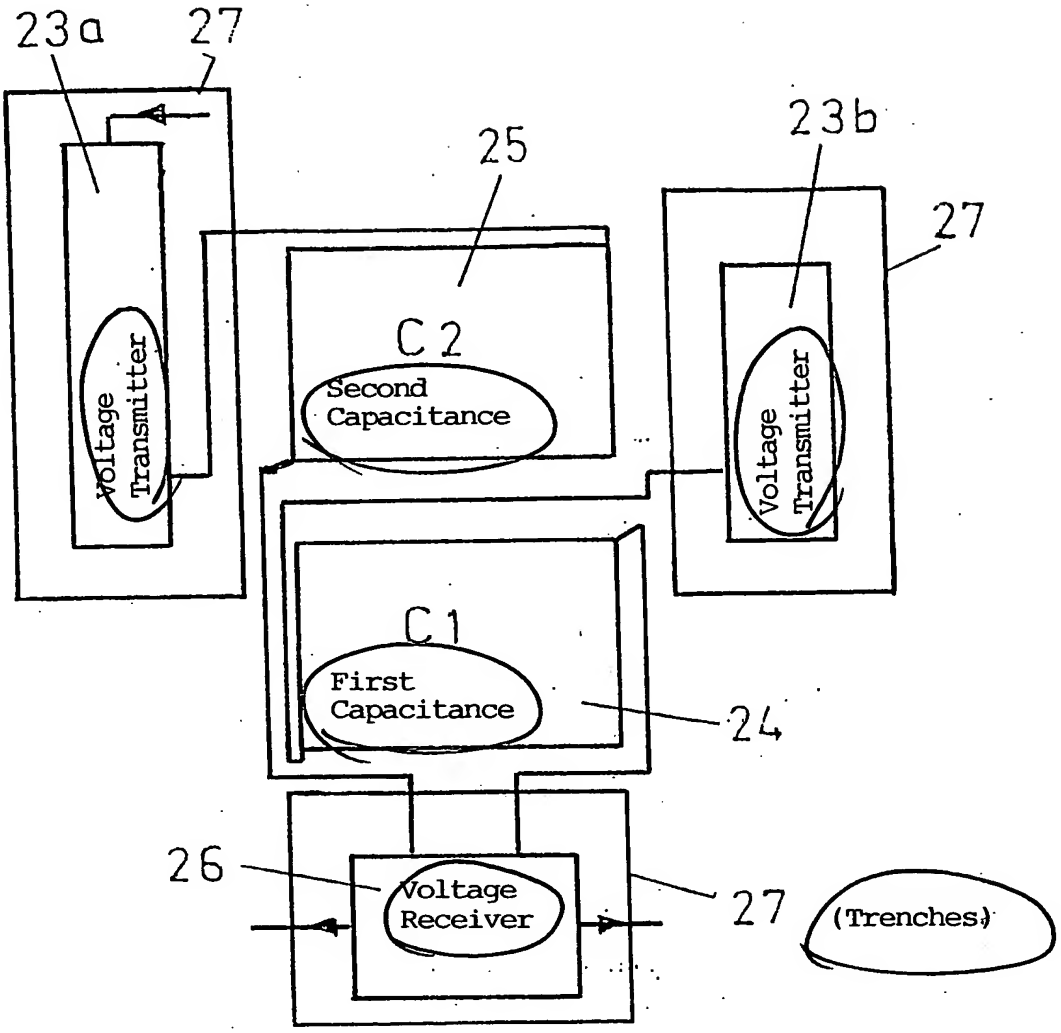


Figure 5

~~Figur 5~~